PHOTOMASK

BACUS—The international technical group of SPIE dedicated to the advancement of photomask technology.

UV NIL template making and imprint evaluation

Shiho Sasaki, Takaaki Hiraka, Jun Mizuochi, Akiko Fujii, Yuko Sakai, Takanori Sutou, Satoshi Yusa, Koki Kuriyama, Masashi Sakaki, Yasutaka Morikawa, Hiroshi Mohri, and Naoya Hayashi, Electronic Device Laboratory, Dai Nippon Printing Co., Ltd. 2-2-1 Fukuoka, Fujimino-shi, Saitama, 356-8507 Japan

ABSTRACT

UV NIL shows excellent resolution capability with remarkable low line edge roughness, and has been attracting pioneers in the industry who were searching for the finest patterns.

We have been focused on the resolution improvement in NIL template making with a 100keV acceleration voltage spot beam EB writer process, and have established a template making process to meet the requirements of the pioneers. Usually such templates needed just a small field (several hundred microns square or so).

Now, for several semiconductor devices, the UV NIL is considered not only as a patterning solution for R&D purpose but eventually as a potential candidate for production, and instead of a small field, a full chip field mask is required. Although the 100kV EB writers have excellent resolution capability, they are adopting spot beams (SB) to generate the pattern and have a fatally low throughput if we need full chip writing.

In this paper, we are focusing on the 50keV variable shaped beam (VSB) EB writers, which are used in current 4X photomask manufacturing. The 50keV VSB writers can generate full chip pattern in a reasonable time, and by choosing the right

Continues on page 3.

Table 1. The requirements on masks.

Year of Production	2013		
DRAM 1/2pitch	32		
Flash 1/2pitch	25		
MPU Gate in resist	21		
DRAM/FRASH CD contol(3 sima)	2.6		
Gate CD control (3sigma)	1.3		
Overlay (3 sigma)	6.4		
MASK Requirement	NIL	EUVL	Optical
Magnification	1	4	4
MASK nominal image size	21	85	85
Image placement (nm, multipoint)	3.7	3.8	3.8/2.7
CDU Isolated lines (MPU gates)	1.2	1.9	1
CDU Dens line DRAM/FRASH(half pitch)	3.1	3.7	1.9
CDU Contact/vias	3.5	2.8	1
Etch depth uniformity	2.1-3.2		
Trench width roughness (3 sigma)	1.9		
Defect size impacting CD x,y	2.5	25	25
Defect size impacting CD z	5.1		

BACUS NEWS

March 2009

Volume 25, Issue 3

TAKE A LOOK INSIDE:

SPIE

EDITORIAL

Is Double Patterning Photomask Deliverable?

Banqiu Wu, Applied Materials, Inc.

Historically, many people in semiconductor industry took it for granted that mask making was straight forward. They believed mask making was never a challenge especially when compared to other lithographic technologies. However, next generation lithography (NGL) proved that masks were difficult to fabricate. Why? Because NGL masks became one of the main failure reasons of NGLs, such as XPL and EPL, or IPL. The question is whether a similar thing will happen with double patterning (DP) technology and EUV lithography.

Double patterning was proposed because it enabled pitch relaxation. Combine pitch relaxation with immersion exposure, and 32- and 22-nm technology nodes seem achievable. Resolution is improved but now the real challenges are transferred to mask making process. When we use one mask to execute the exposure, we require good CD uniformity on the mask. However, when we use two masks to generate one pattern (as with double patterning) we need to control the combined CD of a pair of double-patterning masks; which requires perfect CD Mean to Target (MTT) from the pair DP masks. For example, ITRS requires the difference in CD MTT of two DP masks be smaller than 1.3 nm and 0.9 nm for 32 and 22 nm, respectively.

A current mask fabrication tool set would include a 50 kV e-beam writer, a ICP-bias power plasma etcher, a deep UV inspection tool, a FIB repair tool, and wet-megasonic cleaning tool. These configurations have been used for both 130nm and 90-nm technology nodes. Improvements have been made gradually for every technology node, but there has been no revolutionary progress. The question is: How far can these configurations go? Can these tool sets be used for 32-and 22-nm technology nodes?

Let's break down the CD MTT budgets of mask fabrication processes which affect the final CD values on the masks. For e-beam exposure, the dose is the most important parameter. It is a purely physical parameter and can be relatively accurately controlled. The dose value can be expressed by the "number" of electrons in a unit area. From this perspective, we can say the e-beam writering step is a "digital" process. Another important process in pattern generation is the Post Exposure Bake (PEB). The temperature distribution in PEB plays a critical role in the determination of CD properties. Hopefully, new progress in resist technology will result in reduced PEB influence on CDs.

Patterning the resist layer is just the beginning. The resist image then needs to be transferred into a permanent working layer by pattern transfer, i.e. photomask etch; a specialized gas-solid chemical reaction. Pattern transfer fidelity of the photomask is mainly determined by the resist (a soft mask) and its erosion. The fabrication requires the reaction radicals to be transported to etch surface very accurately and uniformly. Unfortunately, we don't know the reacting components of etch elementary reaction in the etch chamber, as well as we would like to know these reactants, and therefore cannot assure the etching will occur digitally. When compared to writing the mask, etching the mask is not digital process, but it is an analog process.

The greater the resist erosion, occurring in the etch tool, the greater the CD bias and pattern transfer error. The current absorber thickness drives moderate resist consumption, which reduces resist residue which is sometime noticed after photoresist development. In order to reduce resist thickness and erosion, for the purpose of pattern quality control, very thin hard mask layers have been employed. For example, 10-nm thick hard mask and approximately 100-nm thick resist are used for photomasks fabrication. It is expected that by using a

continues on page 7.

BACUS N • E • W • S

BACUS News is published monthly by SPIE for BACUS, the international technical group of SPIE dedicated to the advancement of photomask technology. Circulation 2600.

Managing Editor/Graphics Linda DeLano
Advertising Teresa Roles-Meier
BACUS Technical Group Manager Pat Wight

SPIE

P.O. Box 10, Bellingham, WA 98227-0010 USA
Tel: +1 360 676 3290 or +1 888 504 8171
Fax: +1 360 647 1445
SPIE.org
customerservice@spie.org

N • E • W • S

Continued from cover.

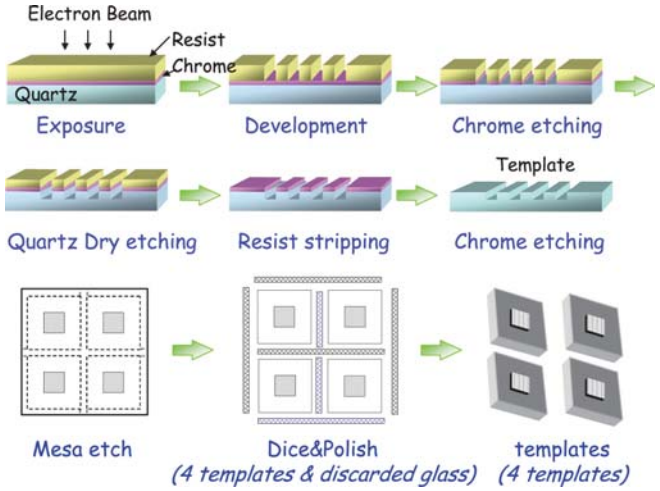


Figure 1. Manufacturing process flow of imprint templates.

Table 2 The experimental tools and materials.

Exposure tool	100keV spot beam EB writer (JBX9300, ELS-7000) 50keV VSB EB writer (4X photomask manufacturing tool)
Resist materials	Non CAR (Positive tone)
Measurements tool	CD-SEM (LWM9000) Image placement measurement (LMS IPRO) Cross section-SEM (Ultra)
Imprint tool	Imprio 250

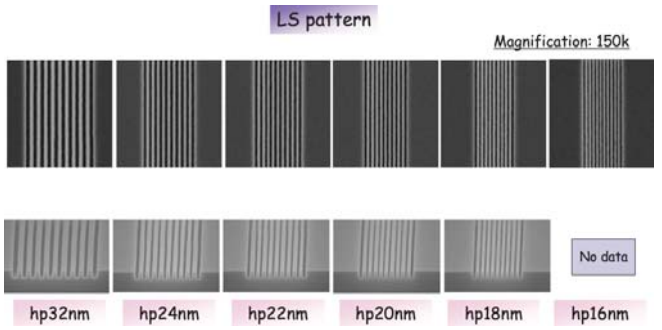


Figure 2. Resolution images of the line and space patterns.

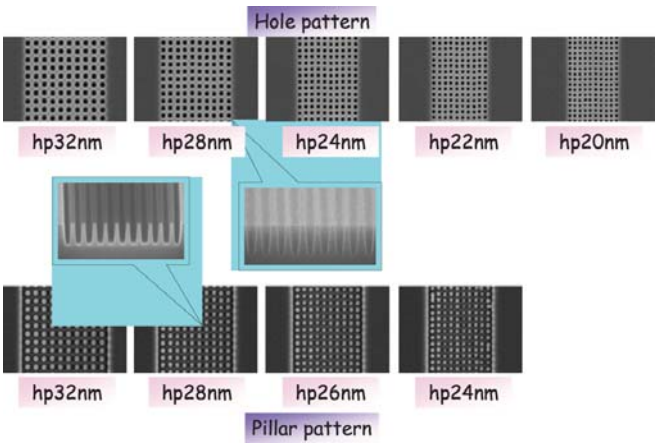


Figure 3. Resolution images of the dense hole and dots.

patterning material and process, we achieved resolution down to 28nm.

1. Introduction

NIL templates have 1X patterns and require patterning process with higher resolution compared to that of the 4X photomasks. Table 1 shows the requirements on masks for NIL, EUV, and optical lithography. Although the patterns on the NIL templates will be made by the EB writing process which will also be used for EUV or photomasks, the resolution should be finer, and close to 20nm in 2013. The defect size requirements are also be tough and are different from other masks, and many efforts should be paid. In this paper we are focusing on the mask resolution, and discussion of defects on mask patterns will be taken up at another papers.

For the NIL template pattern making, we have been evaluating two different processes with 100keV SB EB writer and 50keV VSB EB writer1-4. The 100keV SB writer is for R&D purpose, and has high resolution capability. But it has a fatally low throughput for full field writing. On the other hand, the 50keV VSB writer is actually used in today's advanced photomask manufacturing, and can write full field in a reasonable time. However, they are designed for 4X pattern generation and show relatively low resolution capability compared to the 100keV SB writer.

2. Experimental

Fig. 1 shows our manufacturing process flow of imprint templates. A thin chrome film was coated between the EB resist and the quartz substrate. The thin chrome enabled us to make the resist thickness thinner compared to the 4X photomask resists, and made the resolution remarkably finer. The thin chrome might also reduce charge up problem during EB writing, and decrease resist peeling caused by poor adhesion between resist and quartz.

In general, though the thicknesses are different, the processes are already used in current photomask manufacturing, for example in the manufacturing of alternating PSMs. Only the conditions and parameters are modified to achieve higher resolution.

Table 2 shows the experimental tools and materials. We used the "JBX9300" (JEOL) and "ELS-7000" (Elionix)

Continues on page 4.

Continued from page 3.

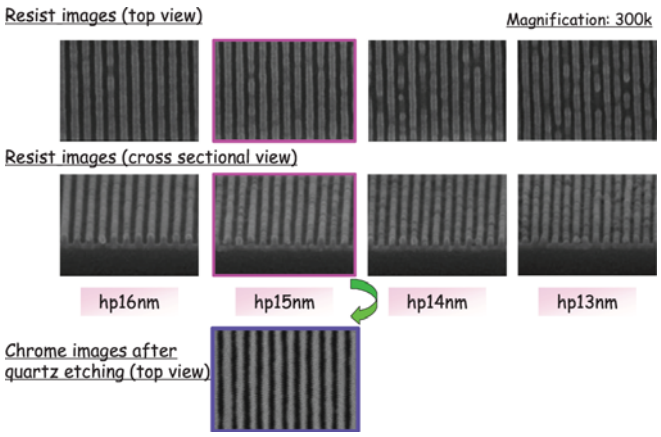


Figure 4. The resist images of our latest improvements.

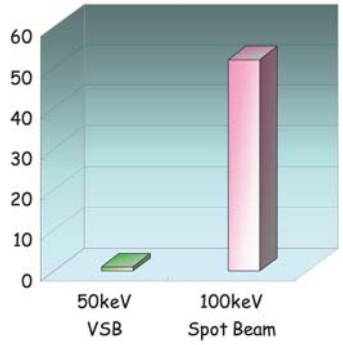


Figure 5. EB writing time comparison.

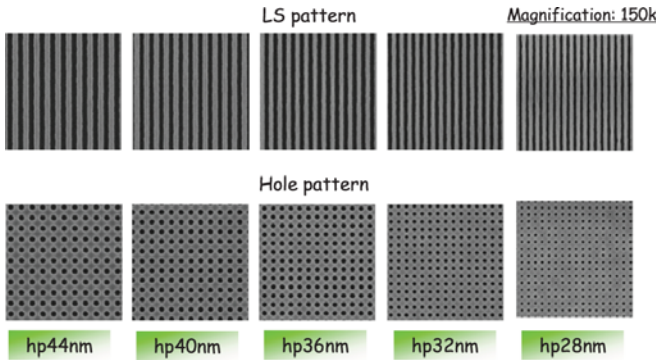


Figure 6. Resolution images of the line and space patterns using 50keV EB writer.

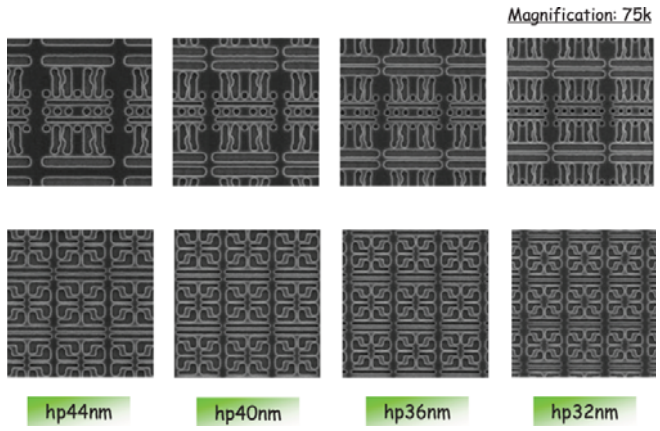


Figure 7. Resolution images of the SRAM patterns using 50keV EB writer.

as the 100keV SB writer. As the 50keV VSB EB writer, machines used in current 4X photomask manufacturing were used. A positive tone non-CAR (non-chemically amplified resist) was used as the resist material. For measurement tools, we used "LWM9000" (Vistec) CD-SEM, "LMS IPRO" (Vistec) image placement measurement tool, and "ULTRA" (Carl Zeiss) SEM. Imprint performance test was done by an "Imprio250" (Molecular Imprints Inc) tool.

3. Results and Discussion

We optimized the process parameters and conditions with the 100keV SB EB writer. Fig. 2 shows the line and space patterns and Fig. 3 shows the dense hole and dots. The resolution limit is hp16nm for line and spaces, hp20nm for dense holes, and hp26nm for dots. Fig. 4 is the resist images of our latest improvements, and shows further resolution for line and spaces, but we can see that around 15nm seems to be the limitation of this process, and we are considering that whether or both of a new resist system and a new writing strategy might be necessary.

Figs. 6 and 7 are templates made with the 50keV VSB writer. The resolution is limited down to hp28nm, but as we can see in Fig. 5, the throughput of the 50keV VSB tool enables to make a larger field. Taking into account that the NIL does not need high load optical proximity correction pattern, the 50keV VSB tool has the potential of NIL template manufacturing.

Figs. 8, 9, and 10 show the critical dimension uniformity (CDU), image placement accuracy, and pattern fidelity of both 50keV VSB and 100keV SB process. CDU and pattern fidelity was evaluated with an hp32nm line and space pattern, so the 100keV SB template shows better results, because of the resolution capability (note that hp32nm is close to limit for the 50keV VSB, while the 100keV SB has still a margin). These performances should be improved to match with the future ITRS requirements, but at this stage of the development, we believe the numbers are acceptable.

To improve the resolution of the 50keV process, along with the CD and image placement accuracy, we are planning to test the newest EB writer which will be

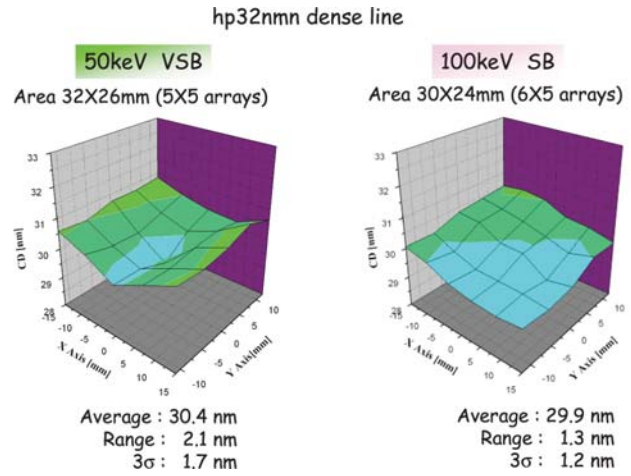


Figure 8. The critical dimension uniformity of both 50keV VSB and 100keV SB process.

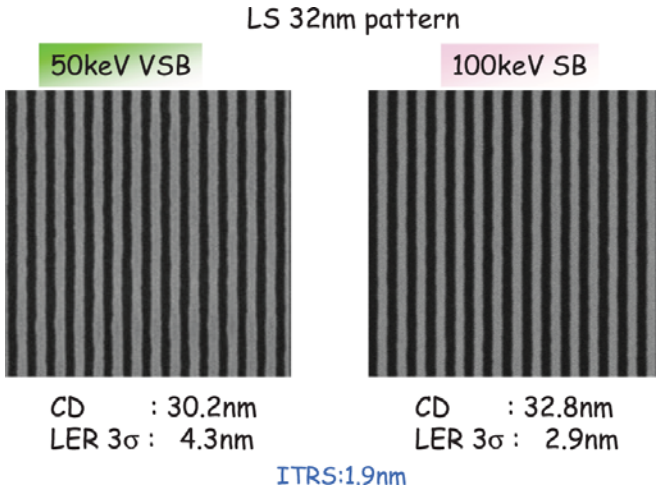


Figure 10. The pattern fidelity of both 50keV VSB and 100keV SB process.

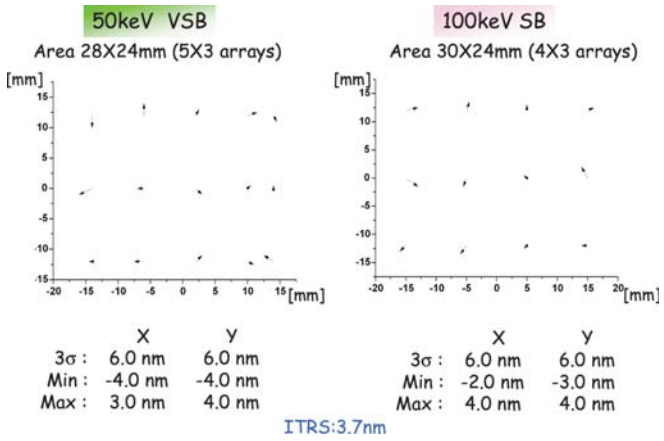


Figure 9. The image placement accuracy of both 50keV VSB and 100keV SB process.

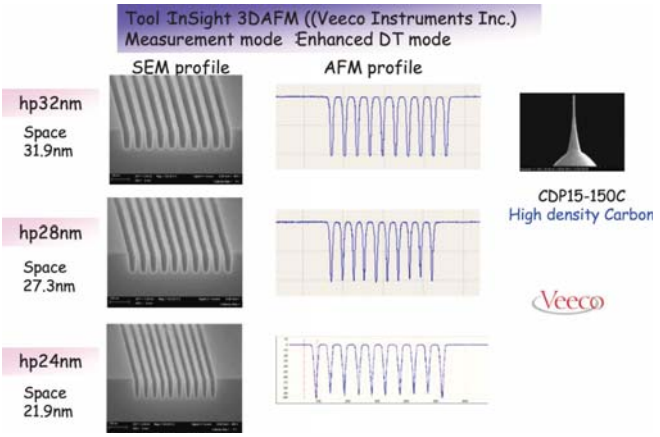


Figure 11. The profile of the template pattern monitored with an AFM.

used for the 32nm node 4x photomasks in the coming years. We have to match the NIL template process, and are planning to collect initial sets of data in the coming months.

Fig. 11 shows the profile of the template pattern monitored with an AFM. An InSight 3D system of Veeco Instruments Inc. was used. A sharp tip made of high density carbon material was used to observe the fine template patterns. We can see that with a commercially available CDP15-150C tip, we can reach the bottom of a 27.3nm space. This could be make the future assurance of the template possible, if not only the planar CD but also the 3D profile of the template pattern have decisive impact on the imprint performance.

Fig. 12 shows the profile monitored with a TEM. A Tecnai G2-F30 of FEI company was used. The TEM photo was taken with the thin chrome on top of the template. The AFM profile should be calibrated with whether the SEM or TEM photo, and our next step should be the discussion of how to do the metrology to assure the template CD, by verifying with the imprint result.

Figs 13 to 16 are the imprint results of our templates. Imprint process and data collection were done by Molecular Imprints Inc.. We can see that the template patterns were well imprinted onto the wafer.

4. Conclusion

NIL template process was discussed focusing on the pattern resolution.

Currently used 50keV VSB EB process has enough capability for full field template manufacturing with patterns down to around hp30nm. To achieve the requirements for the next generation lithography masks, we are

Continues on page 6.

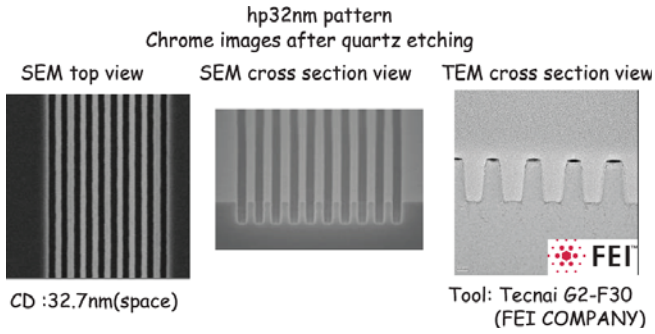


Figure 12. The profile monitored with a TEM.

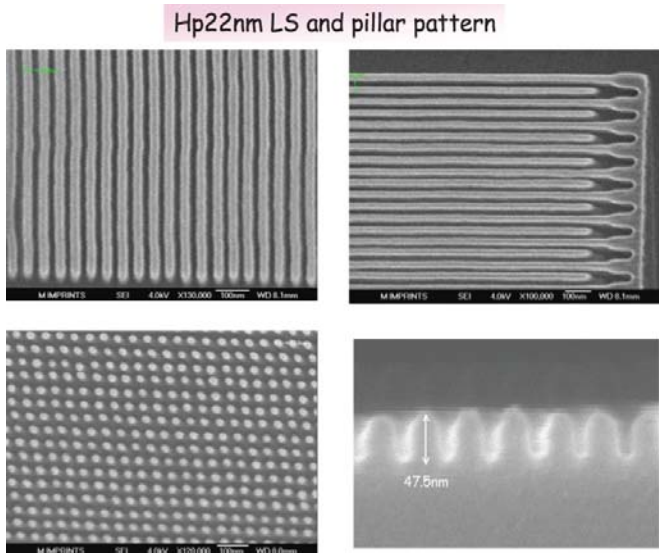
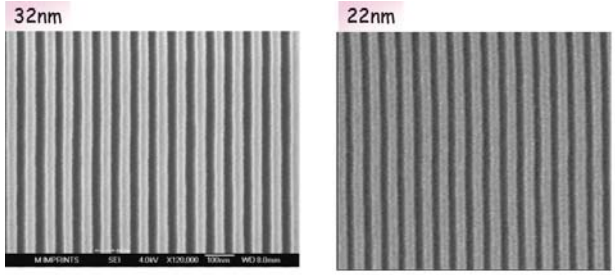


Figure 13. Imprint results using by 100keV template.



Parameter	mean	standard deviation
Line width	31.94	1.84
LWR 3Ξ	2.37	0.36
Pitch	64.10	2.08
LER 3Ξ	2.22	0.30

Parameter	mean	standard deviation
Line width	24.51	0.72
LWR 3Ξ	3.13	0.43
Pitch	44.67	1.51
LER 3Ξ	3.54	0.36

[nm]

Figure 14. Imprint results using by 100keV template.

Continued from page 5.

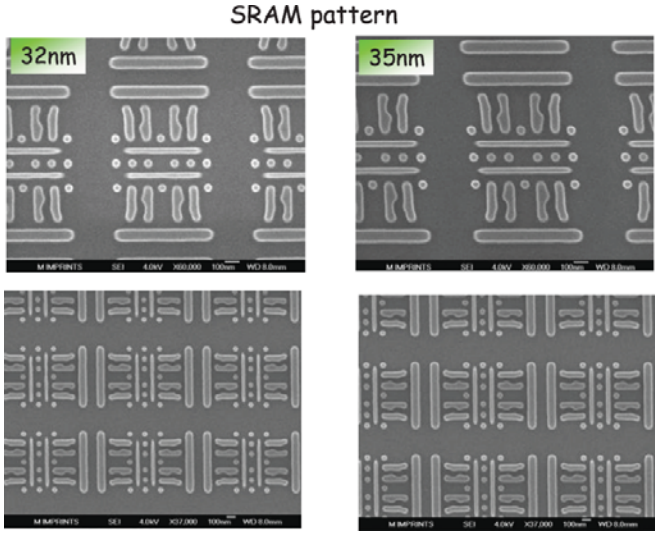
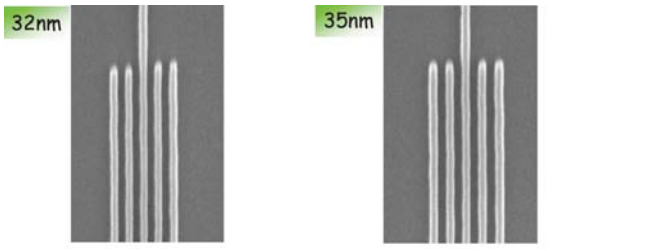


Figure 15. Imprint results using by 50keV template.



Parameter	mean	standard deviation
Line width	33.20	1.70
LWR 3	3.02	0.74
Pitch	66.93	2.37
LER 3	2.26	0.40

Parameter	mean	standard deviation
Line width	35.89	1.85
LWR 3	3.12	0.38
Pitch	71.55	2.82
LER 3	2.08	0.09

[nm]

Figure 16. Imprint LER measurements using by 50keV template.

beginning to test the new 50keV VSB tools designed for the 32nm node 4X photomask manufacturing.

5. Acknowledgment

The authors would like to thank Sean Hand, Max Ho, and Marc Osborn of Veeco Instruments Inc. for the AFM results.

The authors also thank Kaoru Murata and Hiromi Sekiguchi of FEI Company Japan Ltd. for the TEM results and discussion.

Thanks are also due to all Molecular Imprints Inc. people involved, for sharing imprint results.

6. References

1. S. Yusa, T. Hiraka, A. Kobiki, S. Sasaki, K. Itoh, N. Toyama, H. Mohri, and N. Hayashi, "Progress of NIL template making", *Proceeding of SPIE,* Vol. 6607, p. 66073H, 2007.
2. T. Hiraka, S. Yusa, A. Fujii, S. Sasaki, K. Itoh, N. Toyama, M. Kurihara, H. Mohri, and N. Hayashi, "UV-NIL template for the 22nm node and beyond", *Proceeding of SPIE,* Vol. 6730, p. 67305, 2007.
3. S. Yusa, T. Hiraka, J. Mizuochi, A. Fujii, Y. Sakai, K. Kuriyama, M. Sakaki, S. Sasaki, Y. Morikawa, H. Mohri, and N. Hayashi, "Progress of NIL template making", *Proceeding of EMLC2008,* p. 23-34, 2008.
4. A. Fujii, Y. Sakai, J. Mizuochi, T. Hiraka, S. Yusa, K. Kuriyama, M. Sakaki, T. Sutou, S. Sasaki, Y. Morikawa, H. Mohri, and N. Hayashi, "UV NIL mask making and imprint evaluation", *Proceeding of SPIE,* Vol. 7028, p. 70281W, 2008.

EDITORIAL

continued from page 2.

hardmask, DP masks can be fabricated to meet new tighter specifications. However, since very thin resist is consumed during hardmask etch process, imperfection remaining after resist development can be transferred to hardmask, and then into absorber layer. From this standpoint, the hardmask should not be too "hard." Otherwise, defectivity control will be serious issue. This is the conflict between pattern generation and transfer.

For the hardmask perspective, two new challenges have been created. The first challenge is creating a perfect resist pattern without defects or scum. If the low defect low scum challenge is not met a pre-pattern-transfer resist treatment technology will need to be used; this challenge be considered part of the photomask plasma etching process.

DP and EUVL masks may be written by a same writer, but, they will be etched on different mask etchers because of the difference in etched materials. So mask etcher manufacturer, like exposure tool companies, have to spend twice as much on resources, plans, and investment to develop two parallel products for DP and EUVL masks

In conclusion, DP and EUV lithography, will require more cooperation between mask makers, suppliers, and tool makers in order to facilitate the introduction of hardmask technology during photomask manufacturing.

BACUS N • E • W • S

Sponsorship Opportunities

Sign up now for the best sponsorship opportunities for Photomask 2009 and Advanced Lithography 2009. Contact:

Teresa Roles-Meier
Tel: +1 360 676 3290
teresar@spie.org

Advertise in the BACUS News!

The BACUS Newsletter is the premier publication serving the photomask industry. For information on how to advertise, contact:

Teresa Roles-Meier
Tel: +1 360 676 3290
teresar@spie.org

BACUS Corporate Members

Aprio Technologies, Inc.
ASML US, Inc.
Brion Technologies, Inc.
Coherent, Inc.
Corning Inc.
Gudeng Precision Industrial Co., Ltd.
Hamatech USA Inc.
Inko Industrial Corp.
JEOL USA Inc.
KLA-Tencor Corp.
Lasertec USA Inc.
Micronic Laser Systems AB
RSoft Design Group, Inc.
Synopsys, Inc.
Toppan Photomasks, Inc.

Industry Briefs

Good News for the Semiconductor industry and the US: Intel Corp announced it will spend $7 billion over the next two years to build advanced manufacturing facilities in the United States as it looks to 32nm.

By **College of NanoScale Science and Engineering**

The commitment, announced by Intel President and CEO Paul Otellini at the Economic Club of Washington, DC, represents Intel's largest-ever investment for a new manufacturing process and bucks the ongoing trend by many USbased companies to outsource manufcaturing. "We're investing in America to keep Intel and our nation at the forefront of innovation," Otellini said in a statement. "These manufacturing facilities will produce the most advanced computing technology in the world. The capabilities of our 32-nm factories are truly extraordinary, and the chips they produce will become the basic building blocks of the digital world, generating economic returns far beyond our industry."

The announcement comes after the January announcement that Intel would end production at several factories, including its D2 facility in Santa Clara, Calif, and halt production at others, including its Fab 20, a 200mm wafer fabrication facility in Hillsboro, Ore, potentially laying off 6,000 employees in the process. Intel also announced last week that it would shift its China operations, closing a test and assembly plant near Shanghai, moving that capacity to a plant in Chengdu, and impacting 2,000 workers. Both moves were made as the company looked to realign manufacturing to current weak market demand.

Self-assembling polymer arrays improve data storage potential

A new manufacturing approach holds the potential to overcome the technological limitations currently facing the microelectronics and data-storage industries, paving the way to smaller electronic devices and higher-capacity hard drives.

"In the past 20 to 30 years, researchers have been able to shrink the size of devices and the size of the patterns that you need to make those devices, following the use of the same types of lithographic materials, tools and strategies, only getting better and better at it," says Paul Nealey, director of the University of Wisconsin-Madison Nanoscale Science and Engineering Center (NSEC).

Now, those materials and tools are reaching their fundamental technical limits, hampering further performance gains. In addition, Nealey says, extrapolating lithography — a process used to pattern manufacturing templates — to smaller and smaller dimensions may become prohibitively expensive. Further advances will require a new approach that is both commercially viable and capable of meeting the demanding quality-control standards of the industry.

In a collaborative effort between academic and industry, chemical and biological engineering professors Nealey and Juan de Pablo, and other colleagues from the UW-Madison NSEC partnered with researchers from Hitachi Global Storage Technologies to test a promising new twist on the traditional methods. In the Aug. 15 issue of the journal Science, the team demonstrates a patterning technology that may revolutionize the field, offering performance improvements over existing methods even while reducing the time and cost of manufacturing.

The method builds on existing approaches by combining the lithography techniques traditionally used to pattern microelectronics with novel self-assembling materials called block copolymers. When added to a lithographically patterned surface, the copolymers' long molecular chains spontaneously assemble into the designated arrangements.

"There's information encoded in the molecules that results in getting certain size and spacing of features with certain desirable properties," Nealey explains. "Thermodynamic driving forces make the structures more uniform in size and higher density than you can obtain with the traditional materials."

The block copolymers pattern the resulting array down to the molecular level, offering a precision unattainable by traditional lithography-based methods alone and even correcting irregularities in the underlying chemical pattern. Such nanoscale control also allows the researchers to create higher-resolution arrays capable of holding more information than those produced today.

In addition, the self-assembling block copolymers only need one-fourth as much patterning information as traditional materials to form the desired molecular architecture, making the process more efficient, Nealey says. "If you only have to pattern every fourth spot, you can write those patterns at a fraction of the time and expense," he says.

In addition to shared intellectual contributions, the collaboration between the UW-Madison and Hitachi teams provided very clear objectives about creating a technology that is industrially viable. "This research addresses one of the most significant challenges to delivering patterned media — the mass production of patterned disks in high volume, at a reasonable cost," says Richard New, director of research at Hitachi Global Storage Technologies. "The large potential gains in density offered by patterned media make it one of the most promising new technologies on the horizon for future hard disk drives."

In its current form, this method is very well-suited for designing hard drives and other data-storage devices, which need uniformly patterned templates — exactly the types of arrangements the block copolymers form most readily. With additional advances, the approach may also be useful for designing more complex patterns such as microchips.

"These results have profound implications for advancing the performance and capabilities of lithographic materials and processes beyond current limits," Nealey says.

Join the premier professional organization for mask makers and mask users!

About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

Individual Membership Benefits include:

- Subscription to BACUS News (monthly)
- Complimentary Subscription *Semiconductor International* magazine
- Quarterly technical meetings in the Bay Area
- Reduced registration rates at BACUS Photomask Technology annual meeting
- Eligibility to hold office on BACUS Steering Committee

spie.org/bacushome

Corporate Membership Benefits include:

- One Voting Member in the SPIE General Membership
- Subscription to BACUS News (monthly)
- One online SPIE Journal Subscription
- Exhibit Space discount of 8% at either the Photomask or Advanced Lithography Symposium
- Listed as a Corporate Member in the BACUS Monthly Newsletter

spie.org/bacushome

Calendar

2009

Photomask Japan
8-10 April
Hotel Pacifico Yokohama
Yokohama, Japan
www.photomask-japan.org

SPIE Photomask Technology
14-18 September
Monterey Marriott and
Monterey Conference Center
Monterey, California, USA
spie.org/pm

SPIE Lithography Asia - Taiwan
18-20 November
Sheraton Taipei Hotel
Taipei, Taiwan
spie.org/la

Abstracts due 2 June

2010

SPIE Advanced Lithography
21-26 February
San Jose Marriott and
San Jose Convention Center
San Jose, California, USA
spie.org/al

Abstracts due 2 March

You are invited to submit events of interest for this calendar. Please send to lindad@spie.org; alternatively, email or fax to SPIE.

SPIE is an international society advancing light-based technologies.

SPIE

International Headquarters
P.O. Box 10, Bellingham, WA 98227-0010 USA
Tel: +1 888 504 8171 or +1 360 676 3290
Fax: +1 360 647 1445
customerservice@spie.org • SPIE.org

Shipping Address
1000 20th St., Bellingham, WA 98225-6705 USA

SPIE *Europe*

2 Alexandra Gate, Ffordd Pengam, Cardiff,
CF24 2SA, UK
Tel: +44 29 20 89 4747
Fax: +44 29 20 89 4750
spieeurope@spieeurope.org • www.spieeurope.org